 Regulation of 12-pulse Rectifier Converter using ANFIS-based Controller in a HVDC Transmission System

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Abstract. High voltage direct current (HVDC) transmission is a better prospect choice compared to high voltage AC transmission. The HVDC is able to apply higher voltage level and without any reactive power losses. By supporting power electronic technology, the HVDC is simpler and cheaper to be realized. So, the problem in the HVDC system is how to control power flow in rectifier converter device effectively. In this research, regulating of firing delay angle is proposed by ANFIS-based controller (ANC) in 12-pulse rectifier. The ANC is applied because computation of the ANC is more effective than Mamdani fuzzy controller computation. The ANC is trained by data-learning in off-line mode. In normal operation, the maximum transmitted power by the HVDC is on the value of 1.0 pu with voltage and current DC at 1.0 pu when the firing delay angle at 26\textdegree. Also, the ANC is able to compensate temporary short-circuit fault.

Keywords. ANFIS, controller, firing delay angle, HVDC, rectifier.

I. Introduction

High voltage direct current (HVDC) transmission system is usually used to deliver bulk of electric power over a long distance area by overhead conductors or submarine cables. The HVDC system has several advantages compared to high voltage alternating current (HVAC) system such as: location of electric power production are very far from location of consumer, long distance HVDC system do not need reactive power compensation as required by long distance of the HVAC system, to make an asynchronous interconnection and allows more capacity of power to be transmitted/delivered [1] [2]. Also, for a given conductor cross section, the HVDC transmission system can carry more current through this conductor compared to a conventional HVAC system[1].

In order to improve the performance of the HVDC system, some control schemes are applied to its such as: A feedback loop with PI controller is applied to the HVDC. The controller is able to mitigate voltage fluctuation during disturbing condition [3]. Also, PI controller is used to multi-infeed high voltage direct current (MIHVDC). Modified transfer function of HVDC also is introduce with small signal analysis based on linearisation model. Parameters of the PI controller in MIHVDC are optimized using genetic algorithm. The MIHVDC are equipped by PI controller and the optimized parameters are robust during fault condition [4].
Analytical method to calculate the efficiency of two and three-level VSC with average and root mean square of converter current is used to the HVDC system. This method is applied to estimate the losses of DC cable, coupling transformer, AC harmonic filter and conduction – switching at the converter. The analytical method and measuring software technique are compared in order to validate of the results [5]. Moreover, power flow strategy with multi-objective optimization for multi-terminal HVDC grid [6] is done by Carrizosa et al. Line commutated rectifier (LCC) and modular multi-level converter (MMC) are applied in hybrid HVDC topology to clear DC fault. Where, the LCC is adopted as rectifier side and the 2 (two) MMC moduls are adopt as inverter side. This topology is able to block current fault path by alpha-retard (α-retard) of the LCC and high power diode. Also, the system is able to restart after clearance of transient DC line fault [7]. A novel rapid protection whole-line principle to protect the HVDC transmission lines using oneend voltage signal was proposed in [8]. Where, this proposed protection method works by analysing measured voltage of the electric network to identify and distinguish between internal or external faults. Moreover, the proposed method operates rapidly, selectively and with high accuracy, under different fault conditions. Natural frequency of distributed parameter line model is applied to determine the fault location on light HVDC system [9]. Using spectral analysis of current by the proxy algorithm, a short data window is sufficient to detect the natural frequency and fault location accurately. It is found that the accuracy of fault location over entire HVDC transmission line is not affected by fault resistance and fault type.

Some intelligent control such as: Neural network (NN), fuzzy and neuro-fuzzy control are applied successful in electrical and other engineering fields to replace the function of conventional control scheme in recent years. Proportional integral derivative-static var compensator (PID-SVC) based on recurrent NN has been applied to control chaos and voltage collapse in critical loading of a power system [10]. Moreover, ANFIS-based composite controller-SVC and PID-loop have been applied to control chaos, voltage collapse, and to regulate the load voltage at load bus. In this control scheme, the load bus is varied. In order to maintain the load voltage on the setting value, the reactive power compensation is provided by the SVC [11] [12]. ANFIS controller is applied to control and fault identification in converter of HVDC system. Where, this controller is able to improve dynamic response of the system [13]. Furthermore, ANFIS-based power system stabilizer has been applied to improve the stability of single machine based on feedback linearisation [14]. In this research, we focus on controlling rectifier of HVDC using ANFIS-based controller to replace the conventional controller. This paper is organized as follows: High voltage direct current (HVDC) is described in Section II. ANFIS-based rectifier controller design is detailed in Section III. Next, simulation result and analysis are presented in Section IV. And, the conclusion is provided in the last section.

II. HVDC Transmission Model

The advantage of HVDC is the ability to control the transmitted power rapidly. Proper design of the HVDC control is essential to ensure satisfactory performance of the overall AC/DC transmission systems [15]. Some aspects of power flow control in HVDC using flexible AC transmission system are described in [16] [17].

Consider a DC transmission system to be compared with a 3-phase AC system transmitting the same power, having the same percentage losses and using the same size conductor. Where the DC system is considered to have 2 (two) conductors at $V_d$ to earth. These formulas are as follows [1]: Power in the AC system ($P_a = 3E_{ph}I_L$ assumed that $\cos \phi = 1.0$), power in the DC system ($P_d = 2V_dI_d$), AC losses ($3I_d^2R$) and DC losses ($2I_d^2R$). Equating line losses,

$$3I_d^2R = 2I_d^2R$$

Or

$$I_d = \frac{\sqrt{2}}{\sqrt{3}}I_L$$
equating powers,

$$V_{dl} = (\sqrt{3}/\sqrt{2})E_{ph}$$

where $E_{ph}$, $I_L$, $P_a$, $V_{dl}$, $I_d$, $P_d$ and $R$ are the AC voltage phase to neutral, AC line current, 3-phase AC real power, DC voltage, DC current, DC power and line resistance, respectively.

![Diagram of HVDC transmission system](image)

**Fig. 1.** Model of HVDC transmission system

The HVDC model in this research is taken from [18] and is shown in Fig. 1. The system consist of 4 buses, step-up/down transformer, 3-phase rectifier/inverter, $R_L$ series branch and 300 km long HVDC transmission. Bus parameters are as follows: Bus 1 consist of AC source with third harmonic, 5000 MVA equivalent, 500 kV, 80°, 60 Hz. Bus 2: (Capacitor bank + 11th + 13th + 24th harmonic filters)x150 MVAR and 3-phase rectifier. Bus 3: Three-phase inverter and 150 MVARx(capacitor bank + 11th + 13th + 24th harmonic filters). And, Bus 4: AC source with third harmonic, 1000 MVA equivalent, 345 kV, 80°, 50 Hz. Branch parameters: AC line 1 26.07 and 48.86x10⁻³ H. The transmission DC line: 6.5, 1.2376 H and 4.32x10⁻⁶ F. And, the transmission AC line 2: 6.205 and 13.96x10⁻³ H.

### III. ANFIS-Based Control Design

**Rectifier Converter and Its Controller**

Rectifier converter is very important in HVDC system, that the rectifier converter is used to convert alternating current (AC) to direct current (DC). Therefore, the DC will be transmitted from sending-end to receiving-end through HVDC transmission system. Fig. 2 shows the 12-pulse firing controller unit of the rectifier converter. The controller unit produced $Pulse_Y$ to trigger the respective thyristor-gate at 3-phase $A,B,C$ in star (Y) connected. Also, this controller unit produced $Pulse_\Delta$ to fire respective thyristor-gate at 3-phase $A,B,C$ in delta (Δ) connected. Moreover, the voltage/current from the both star and delta connected were used to generate DC voltage ($V_{dl}$) and current ($I_d$) in the DC side of the rectifier. In order to regulate the level of voltage/current rectifier converter is proper to appropriate of demand side needed, it is convenient to provide this rectifier converter by the controller unit.

![Diagram block of the HVDC rectifier](image)

**Fig. 2.** Diagram block of the HVDC rectifier
The main function of rectifier controller unit is to produce firing delay angle ($\alpha_{ord}$) signal. This signal is fed to the 12pulse firing control of the respective thyristor-valve in bridge converter. So, the 12-pulse firing controller generates trigger pulse, that this trigger pulse is used to on/off the thyristor-gate. Furthermore, this controller also produces two other output signals such as: Reference current ($I_{ref}$) and mode operation (Mode) of rectifier. The diagram block of conventional rectifier controller is shown in Fig. 3(a). Reference current ($I_{ref}$) is used as the target current level of rectifier, where the DC line current ($I_d$) should follow the ($I_{ref}$) on every time. And, the control mode is used to classify the operation of the rectifier into Mode 0: blocked mode, 1: current, 2: voltage , 3: $a_{min}$, 4: $a_{max}$, 5: forced $a$ and Mode 6: $y$ mode.

Fig. 3. Diagram block of 12-pulse rectifier controller

**Training of ANFIS-based Controller**

Before ANFIS-based controller (ANC) is applied to the HVDC converter, that the ANC is trained in some training processes. The data that used on training process were obtained by simulating the conventional controller. The conventional controller is shown in Fig. 3(a). On this training process, a 4000-data point was used to learn the ANFIS controller. Input of the ANC was 5 (five) input variables such as: $V_{dlc}$, $I_d$, $I_{ref}$, block and forced $a$. Three (3) ANFIS models were used to implement the rectifier controller such as: ANFIS1, ANFIS2 and ANFIS3. The output of respective ANFIS model were the $a_{ord}$, $I_{ref}-R$ and mode operation of the rectifier (Mode R). The ANC diagram block of the rectifier converter is shown Fig. 3(b).

In this research only the ANFIS1 topic is described, meanwhile ANFIS2 and ANFIS3 are not discussed. Structure of ANFIS controller was built by 5 (five) inputs Sugeno fuzzy model and 1 (one) output as shown in Fig. 4(a). The training process was conducted in off-line session and subtractive clustering method was used to generate fuzzy inference system (FIS). In this session, some parameters such as: Range of influence = 0.5, squash factor = 1.5, accept ratio = 0.5 and reject ratio = 0.15 were taken. Every input variables were consist of 4 (four) Gaussian membership functions, the $I_d$ input was taken as example and shown in Fig. 4(b). After some training processes were conducted, control surface of respective input-output controller was obtained automatically. This session produced ten (10) sets of input-output control surface of the ANC. An example of the input-output control surface is a DC line voltage-DC current-firing delay ($V_{dlc}$-$I_d$-$a_{ord}$). So, this control surface is shown in Fig. 4(c).
Table 1. Performance Of Anfis Controller At Normal Operation

<table>
<thead>
<tr>
<th>period/observed</th>
<th>$t_0$ (0.2 s)</th>
<th>$t_1$ (0.3 s)</th>
<th>$t_2$ (1.4 s)</th>
<th>$t_3$ (1.6 s)</th>
<th>$t_4$ (1.7 s)</th>
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</thead>
<tbody>
<tr>
<td>$\alpha_{c_1,d}$</td>
<td>90.0-</td>
<td>92.0-</td>
<td>26.0-</td>
<td>166.0</td>
<td>166.0</td>
</tr>
<tr>
<td>$\alpha_{c_2,d}$</td>
<td>92.0</td>
<td>30.0</td>
<td>40.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{p/[p-p]}$</td>
<td>1.135</td>
<td>1.135</td>
<td>0.96</td>
<td>1.135</td>
<td>1.135</td>
</tr>
<tr>
<td>$I_{L_{c_2,p-p}}$</td>
<td>0.96</td>
<td>1.135</td>
<td>0.99</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{c_2,p-p}$</td>
<td>0.5</td>
<td>0.5</td>
<td>11.9</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>$V_{d,r}$</td>
<td>0.05-</td>
<td>1.06-</td>
<td>1.0</td>
<td>0.96</td>
<td>-0.25</td>
</tr>
<tr>
<td>$P_{d,r}$</td>
<td>1.06</td>
<td>1.0</td>
<td>0.96</td>
<td>-0.25</td>
<td>0.0</td>
</tr>
<tr>
<td>$I_d$</td>
<td>0.04</td>
<td>0.04</td>
<td>1.0</td>
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<tr>
<td>$P_d$</td>
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<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
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</tr>
</tbody>
</table>

IV. Simulation and Analysis

To demonstrate the performance and applicability of the proposed controller, the HVDC system equipped by that controller was examined using Matlab/Simulink 7.9.0.529 (R2009b) [19] on an Intel Core 2 Duo E6550 233 GHz PC computer and windows 7 64-bit (win64) operating system. The simulations were done as follows:

A. Performance of ANFIS-based Controller at Start/stop and Ramp-up/down

Scenario 1: the HVDC system was operated with some parameter as follows: At start-up both converters were deblocked and ramped-up to the minimum current (minimum steady-state current reference, MSCR) at 0.1 pu with an adjustable rate (start ramp rate, SRR) and application time (start ramp time, SRT) at 0.3333 pu/s and 0.02 s, respectively. Next, after the system stabilization the current was ramped-up to its final value (up-ramp final value, UFV) with an adjustable rate (up-ramp rate, UR) and execution time (up-ramp time, UT) at the final value of 1.0 pu, 9.0 pu/s and time of 0.3 s, respectively. Before stopping the converters (at stop time, ST) the current was ramped-down to the minimum current with an adjustable rate (down-ramp rate, DR) and execution time (down-ramp time, DT) at the value of -9.0 pu/s and at the time of 1.4 s, respectively. Finally, at stop time the reference was ramped-down to zero value at time of 1.6 s with the same rate used for the start ramp.
Fig. 5(a) and Table I show the firing delay angle ($\alpha_{\text{ord}}$) control at this scenario. In this graphical result the $\alpha_{\text{ord}}$ for conventional controller (CVC) was added by 20° to differentiate the $\alpha_{\text{ord}}$ from the ANC result. It is shown that the $\alpha_{\text{ord}}$ was started at 90°. Next, the $\alpha_{\text{ord}}$ increased to 92° at time $t_0$.

So, the $\alpha_{\text{ord}}$ decreased to 30° at time $t_1$ and decreased again to 26° until time 1.2 s. The $\alpha_{\text{ord}}$ increased to 40° at time $t_2$, and increased again to 166° at time $t_3$. Fig. 5(b) shows the mode operation of rectifier in this scenario. Firstly, the rectifier was operated in Blocked Mode from time 0.0 s until time $t_0$, and the Blocked Mode operation was changed to Current Mode at time $t_0$ until 1.1 s. So, at time 1.1 s the rectifier was operated $\alpha_{\text{min}}$ Mode until time 1.25 s. Next, the rectifier was on Current Mode again until time $t_1$ and at time $t_1$ the rectifier operated was on Forced $\alpha$ Mode until $t_4$. Finally, the rectifier was operated at Blocked Mode from time $t_4$ to infinite time.

Fig. 6(a) and Table II show that $V_{dc}$ increased at the values from 0.05 to 1.06 pu at times from $t_0$ to $t_1$, respectively. So, the $V_{dc}$ decreased from 1.06 to 1.0 pu at times from $t_1$ to $t_2$. Next, the $V_{dc}$ decreased again from 1.0 to 0.96 pu at times from $t_2$ to $t_3$, respectively. Finally, the $V_{dc}$ decreased again from 0.96 to 0.25 pu at times from $t_3$ to $t_4$. Fig. 6(b) shows DC line current ($I_d$) compared to reference current ($I_{\text{ref}}$). Firstly, at time $t_0$ the $I_d$ was at the value of 0.04 pu until time $t_1$. So, the $I_d$ increased from 0.04 to 0.4 pu at time 4.0 s and increased again from 0.4 to 1.0 at time from 0.4 to 0.6 s. This $I_d$ still at the value of 1.0 until $t_2$. And, the $I_d$ decreased from 1.0 to 0.0 pu at times from $t_2$ to $t_3$.

![Fig. 6. The DC line voltage and current at normal operation.](image)

Simulation shows that some results of proposed controller (ANC) in this scenario such as: Firing delay control, mode operation, voltage/current AC input and direct voltage/current output of rectifier are similar to the results of conventional controller (CVC). According to simulation results of the ANC, it is potential to replace the CVC by using ANC permanently. Moreover, to explore ability of the ANC on the HVDC at disturbances/faults condition that the topic will be explained in Scenario 2.

**B. Performance of the Controller to cover disturbance/fault**

Scenario 2: Four temporary disturbances/faults were forced to the HVDC system on different time. Location and time duration of the respective disturbance/fault are illustrated in Fig. 7. Control strategy of the rectifier to cover disturbance/fault is conducted by regulating the firing delay angle ($\alpha_{\text{ord}}$) and by switching mode operation of this rectifier. Graphical visualization of the $\alpha_{\text{ord}}$ and mode operation are illustrated in Figs. 8(a) and (b), respectively. Firstly, positive pole to ground fault occurred at point $F_1$ of HVDC line from time 0.5 ($t_{10}$) to 0.6 s ($t_{11}$). The $\alpha_{\text{ord}}$ was regulated to the value of 16.5° at time $t_{10}$, and decreased to 16.2° from $t_{11}$ until before $t_{12}$. Next disturbance, decreasing of reference current was occurred ($F_2$) at the value of −0.25 pu from time 0.75 $t_{12}$ to 0.85 s ($t_{13}$).
In this condition, the $\alpha_{ord}$ increased sharply to 38.6° at time $t_{12}$, then at a moment it was decreased to 16.9° until time $t_{13}$. From time $t_{13}$ to time a moment before 1.0 s ($t_{14}$) it was oscillated from 16.9° to 10.7°. Positive pole to ground fault occurred at point $F_1$ from time $t_{14}$ to 1.1 s ($t_{15}$), the $\alpha_{ord}$ decreased to 8.0° at time $t_{15}$, the $\alpha_{ord}$ was increased to 11.0° at time $t_{15}$, then increased again to 12.0° before the time 1.2 s ($t_{16}$). Finally, three-phase fault to ground occurred at AC line2 ($F_4$) from $t_{16}$ to 1.3 s ($t_{17}$), the $\alpha_{ord}$ increased to 12.0° at time $t_{16}$, so the $\alpha_{ord}$ stayed at this value until time $t_{17}$. Completeness numerical result of the firing delay angle is listed in Table II.

Fig. 7. The HVDC system is forced by disturbances/faults at F1, F2, F3 and F4 points.

From Fig. 8(b), it is shown that the rectifier was operated on $\alpha_{min}$ Mode at time from 0.0 s to 0.2499 s. From time 0.25 to 0.5299 s the rectifier operation was changed to Current Mode, then the rectifier operation was changed again to $\alpha_{min}$ Mode from time 0.53 to 0.5499 s. Next, from time 0.55 to 0.9099 the rectifier was on Current Mode, and it was in $\alpha_{min}$ or Mode Current alternately.

Fig. 9(a) shows the pattern of three-phase voltage input ($V_{ph}$) of rectifier. The voltage input varied from 0.99 to 0.92 pu for upper limit and lower limit, respectively. Dynamical of three-phase current input ($I_{ph}$) is shown in Fig. 9(b) and listed in Table II. It is shown that the $I_{ph}$ was at the value of 11.3 pu at time $t_{10}$, this current increased to 11.89 pu at time $t_{11}$ and increased again to 11.95 until time $t_{12}$. At time $t_{12}$, this current decreased from 11.95 to 9.01 pu at time $t_{13}$. At time $t_{13}$, this current oscillated in range of 11.0 - 11.20 pu until time $t_{14}$. From time $t_{14}$, $t_{15}$, $t_{16}$, and $t_{17}$ this current increased from 11.10 to 11.20, 11.60, and 12.01 pu, respectively.
Fig. 9. Dynamical of AC input voltage and current.

Fig. 10(a) shows the pattern of DC line voltage ($V_{dc}$) for the conventional controller (CVC) and ANFIS-based controller (ANC). It is shown that the time at $t_{10}$, the $V_{dc}$ was at the value of 1.0 pu, then this voltage decreased moderately to 0.99 and 0.98 pu at time $t_{11}$ and until time $t_{12}$. At time $t_{12}$, this voltage decreased sharply to 0.822 pu, at a moment this voltage increased to 0.975 pu until time $t_{13}$. So, at time $t_{13}$ this voltage increased sharply again to 1.15 pu and at a moment this voltage decreased and oscillated to 0.935 pu until $t_{14}$. At time $t_{14}$ this voltage increased to 1.09 pu until time $t_{15}$, then this voltage decreased to 1.05 pu until time $t_{16}$. This voltage decreased again to 1.02 pu at time $t_{16}$ and stayed in this voltage until $t_{17}$.

Dynamical of the reference current ($I_{ref}$), DC current ($I_d$) for the CVC and ANC are illustrated in Fig. 10(b). From Fig. 10(b) and Table II, it is shown that the $I_d$ was at the value of 1.013 pu for time $t_{10}$, so the $I_d$ decreased at a moment to 0.995 from time $t_{11}$ to time $t_{12}$. Next, at time $t_{12}$ the $I_d$ decreased sharply to 0.775 pu, then it increased moderately to 0.780 until time $t_{13}$. At time $t_{13}$, the $I_d$ increased and oscillated from 0.78 to 0.94 pu until time $t_{14}$, and at time $t_{14}$ the $I_d$ decreased to 0.77. Then, it increased to 0.945 and increased again to 0.948 pu for time $t_{15}$ and time $t_{16}$, respectively. Finally, at the time $t_{16}$ the $I_d$ increased from 0.948 to 1.01 pu until time $t_{17}$. Simulation results in this scenario show that the DC currents produced by the CVC and ANC are able to follow the given reference current. The both controllers are working properly and they are giving good performances. Although, the $I_d$ response of the ANC is still oscillate in severe disturbance case such as: When current reference is reduced to $-0.25$ pu ($F_2$). Some control strategies should be applied to improve the rectifier performance and to anticipate the $I_d$ oscillation response when the rectifier is operated in severe disturbances/faults.

Table II Performance Of The Controller At Disturbances/Faults

<table>
<thead>
<tr>
<th>Period (time)</th>
<th>$t_{10}$ (0.5 s)</th>
<th>$t_{11}$ (0.6 s)</th>
<th>$t_{12}$ (0.75 s)</th>
<th>$t_{13}$ (0.85 s)</th>
<th>$t_{14}$ (1.0 s)</th>
<th>$t_{15}$ (1.1 s)</th>
<th>$t_{16}$ (1.2 s)</th>
<th>$t_{17}$ (1.3 s)</th>
</tr>
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<tbody>
<tr>
<td>$\alpha_{ref}$ (°)</td>
<td>10.7</td>
<td>16.5-16.2</td>
<td>16.2-38.5</td>
<td>38.6-18.9</td>
<td>16.9-3.0</td>
<td>8.0-11.0</td>
<td>11.3-12.8</td>
<td>12.0</td>
</tr>
<tr>
<td>$V_{dcl}(pu)$</td>
<td>0.965</td>
<td>0.985-0.945</td>
<td>0.93-0.99</td>
<td>0.9-0.92</td>
<td>0.96-0.98</td>
<td>0.975-0.965</td>
<td>0.968-0.961</td>
<td>0.966</td>
</tr>
<tr>
<td>$I_{dcl}(pu)$</td>
<td>1.1</td>
<td>11.89-11.95</td>
<td>11.95-0.01</td>
<td>9.01-11.10</td>
<td>11.10-11.20</td>
<td>11.26-11.60</td>
<td>11.60-12.01</td>
<td>12.01</td>
</tr>
<tr>
<td>$I_{d}(pu)$</td>
<td>1.0</td>
<td>0.999-0.986</td>
<td>0.822-0.975</td>
<td>1.25-0.33</td>
<td>0.935-0.19</td>
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<td>0.935-0.19</td>
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<tr>
<td>$P_{d}(pu)$</td>
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<td>0.895-0.775</td>
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V. Conclusion

In this research ANFIS-based controller (ANC) is proposed to regulate the firing delay angle of 12-pulse rectifier HVDC. The ANFIS controller is implemented because computation complexity of the ANFIS controller is more efficient than that of fuzzy Mamdani controller. The ANC is built by training processes in off-line session with subtractive clustering method to generate membership function automatically. So, data training of the learning session are provided by simulating the HVDC with conventional controller in varied condition operations. During the learning processes, a 4000-point data set is used to learn the ANC controller per session. The structure of the ANC is built by five signal inputs (DC line voltage, DC current, reference current, block and forced α), and a firing delay angle signal as an output. The respective input of the ANFIS-based controller is represented by Gaussian membership function. Moreover, the output is described by linear membership function. Performance of the ANC is observed on the firing delay angle, mode operation, AC voltage/current input, DC line voltage, and DC current responses, respectively. Simulation results show that the maximum power conversion is 1.0 pu at the firing delay angle 26°, the DC voltage and current are at the values of 1.0 pu when the HVDC operated in normal condition. Furthermore, the ANC is also able to cover temporary short circuit AC/DC fault on the HVDC. Meanwhile, the ANC responses are still oscillate when the reference current is reduced. Some efforts should be done to damp the oscillation in the next research.

References


